Please amend the present application as follows:

***Claims***

The following is a copy of Applicants' claims that identifies language being added with underlining ("___") and language being deleted with strikethrough ("——"), as is applicable:

1. (Previously presented) A frequency synthesizer circuit, comprising:

a controllable oscillator configured to generate an output signal having a predefined frequency, the controllable oscillator having a plurality of operational states responsive to a plurality of control signals, each of the plurality of operational states defining a distinct frequency for the output signal of the controllable oscillator; and

a frequency control circuit in communication with the controllable oscillator, the frequency control circuit configured to determine the distinct frequency for the output signal that best approximates the predefined frequency and to provide the plurality of control signals, the plurality of control signals configured to change the controllable oscillator to the operational state corresponding to the distinct frequency that best approximates the predefined frequency, wherein the frequency control circuit comprises a frequency detector configured to determine the frequency of the output signal, a comparator configured to compare the frequency of the output signal to the predefined frequency, and logic configured to determine which of the plurality of distinct frequencies for the output signal corresponding to the plurality of operational states best approximates the predefined frequency.

2. (Previously presented) The circuit of claim 1, further comprising a switch, wherein the logic is configured to activate the switch to enable either fine tune frequency control or coarse frequency control.

3. (Original) The circuit of claim 1, wherein the controllable oscillator comprises a plurality of parallel capacitors capable of being engaged by the plurality of control signals, the plurality of parallel capacitors defining the plurality of operational states of the controllable oscillator.

4. (Original) The circuit of claim 1, wherein the logic implements a binary search algorithm to determine which of the plurality of distinct frequencies for the output signal corresponding to the plurality of operational states best approximates the predefined frequency.

5. (Currently Amended) The circuit of claim 1, wherein the frequency control circuit further comprises:

a program counter configured to generate a timing signal based on the predefined frequency, the timing signal having a plurality of clock pulses;

the frequency detector configured to receive the timing signal and, in response to each of the plurality of clock pulses, to generate a first digital word corresponding to the current frequency of the output signal of the controllable oscillator;

a digital decoder configured to receive information, the information associated with the predefined frequency of the output signal of the controllable oscillator, and to generate a second digital word corresponding to the predefined frequency;

the comparator configured as a digital comparator configured to compare the first digital word to the second digital word; and

the logic configured to receive the timing signal and, in response to each of the plurality of clock pulses, to generate the plurality of control signals based on the comparison of the first digital word to the second digital word.

6. (Previously presented) A communication device for use in a communication system, comprising:

a transceiver configured to communicate with the communication system via a communication channel at a channel frequency; and

a frequency synthesizer configured to select the communication channel, the frequency synthesizer comprising:

a controllable oscillator configured to generate an output signal having a predefined frequency corresponding to the channel frequency, the controllable oscillator having a plurality of operational states responsive to a plurality of control signals, each of the plurality of operational states defining a distinct frequency for the output signal of the controllable oscillator; and

a frequency control circuit in communication with the controllable oscillator, the frequency control circuit configured to determine the distinct frequency for the output signal that best approximates the predefined frequency and to provide the plurality of control signals, the plurality of control signals configured to change the controllable oscillator to the operational state corresponding to the distinct frequency that best approximates the predefined frequency, wherein the frequency control circuit comprises a frequency detector configured to determine the frequency of the output signal, a comparator configured to compare the frequency of the output signal to the predefined frequency, and logic configured to determine which of the plurality of distinct frequencies for the output signal corresponding to the plurality of operational states best approximates the predefined frequency.

7. (Previously presented) A method for controlling the frequency of an output signal of a controllable oscillator, the controllable oscillator having a plurality of operational states, each of the plurality of operational states defining a distinct frequency for the output signal of the controllable oscillator, the method comprising:

receiving information associated with a predefined frequency;

generating a timing signal based on the predefined frequency, the timing signal having a plurality of clock pulses;

responsive to each of the plurality of clock pulses, generating a first digital word corresponding to a current frequency of the output signal of the controllable oscillator;

generating a second digital word corresponding to the predefined frequency;

comparing the first digital word to the second digital word; and

generating a control signal to change the controllable oscillator to the operational state corresponding to the distinct frequency that best approximates the predefined frequency based on the comparison of the first digital word to the second digital word.

8. (Currently Amended) The method of claim 7, wherein ~~the~~ generating the control signal ~~comparing~~ comprises executing a binary search algorithm.

9. (Original) The method of claim 8, further comprising changing the controllable oscillator to the operational state corresponding to the distinct frequency that best approximates the predefined frequency.

10. (Original) The method of claim 9, wherein the changing the controllable oscillator to the operational state corresponding to the distinct frequency that best approximates the predefined frequency involves configuring a plurality of parallel capacitors in a predetermined manner.

11. (Original) A method for controlling the frequency of an output signal of a controllable oscillator, the controllable oscillator having a plurality of operational states, each of the plurality of operational states defining a distinct frequency for the output signal of the controllable oscillator, the method comprising:

receiving information associated with a predefined frequency;

determining a current frequency of the output signal of the controllable oscillator, the current frequency corresponding to a current operational state;

comparing the predefined frequency to the current frequency;

based on the comparing the predefined frequency to the current frequency, selecting one of two next operational states, the selected next operational state having a distinct frequency which better approximates the predefined frequency.

12. (Original) The method of claim 11, further comprising generating a control signal configured to change the controllable oscillator to the selected next operational state.

13. (Original) The method of claim 12, further comprising changing the controllable oscillator to the selected next operational state.

14. (Original) The method of claim 13, wherein the changing the controllable oscillator to the selected next operational state involves configuring a plurality of parallel capacitors in a predetermined manner.

15. (Previously presented) The method of claim 13, further comprising repeating the determining the current frequency of the output signal of the controllable oscillator, the comparing the predefined frequency to the current frequency, the selecting one of two next operational states, the generating ~~a~~ the control signal configured to change the controllable oscillator to the selected next operational state, and the changing the controllable oscillator to the selected next operational state.

16. (Currently Amended) A frequency synthesizer circuit, comprising:

a controllable oscillator configured to generate an output signal having a predefined frequency, the controllable oscillator having a plurality of operational states responsive to a plurality of control signals, each of the plurality of operational states defining a distinct frequency for the output signal of the controllable oscillator; and

a frequency control circuit in communication with the controllable oscillator, the frequency control circuit configured to determine the distinct frequency for the output signal that best approximates the predefined frequency and to provide the plurality of control signals, the plurality of control signals configured to change the controllable oscillator to the operational state corresponding to the distinct frequency that best approximates the predefined frequency, wherein the frequency control circuit comprises a program counter configured to generate a timing signal based on the predefined frequency, the timing signal having a plurality of clock pulses, a frequency detector configured to receive the timing signal and, in response to each of the plurality of clock pulses, to generate a first digital word corresponding to ~~the~~ a current frequency of the output signal of the controllable oscillator, a digital decoder configured to receive information, the information associated with the predefined frequency of the output signal of the controllable oscillator, and to generate a second digital word corresponding to the predefined frequency, a digital comparator configured to compare the first digital word to the second digital word, and logic configured to receive the timing signal and, in response to each of the plurality of clock pulses, to generate the plurality of control signals based on the comparison of the first digital word to the second digital word.

17. (Currently Amended) The ~~system~~ circuit of claim 16, wherein the logic is configured to execute a binary search algorithm.

18. (Currently Amended) The ~~system~~ circuit of claim 17, wherein the frequency control circuit is configured to change the controllable oscillator to the operational state corresponding to the distinct frequency that best approximates the predefined frequency.

19. (Currently Amended) The ~~system~~ circuit of claim 18, further comprising a plurality of parallel capacitors communicatively coupled to the frequency control circuit, wherein the plurality of parallel capacitors are configured in a predetermined manner.

20. (Previously presented) A system for controlling the frequency of an output signal of a controllable oscillator, the controllable oscillator having a plurality of operational states, each of the plurality of operational states defining a distinct frequency for the output signal of the controllable oscillator, the system comprising:

means for receiving information associated with a predefined frequency;

means for determining a current frequency of the output signal of the controllable oscillator, the current frequency corresponding to a current operational state;

means for comparing the predefined frequency to the current frequency; and

means for selecting, based on the comparing the predefined frequency to the current frequency, one of two next operational states, the selected next operational state having a distinct frequency which better approximates the predefined frequency.

21. (Original) The system of claim 20, further comprising means for generating a control signal configured to change the controllable oscillator to the selected next operational state.

22. (Original) The system of claim 21, further comprising means for changing the controllable oscillator to the selected next operational state.

23. (Original) The system of claim 22, wherein the means for changing the controllable oscillator to the selected next operational state comprises a plurality of capacitors configured in a predetermined manner.

24. (Currently Amended) The system of claim 22, further configured to repeat the determining the current frequency of the output signal of the controllable oscillator, the comparing the predefined frequency to the current frequency, the selecting one of two next operational states, the generating ~~a~~ the control signal configured to change the controllable oscillator to the selected next operational state, and the changing the controllable oscillator to the selected next operational state.

25. (Currently Amended) A computer readable medium for controlling the frequency of an output signal of a controllable oscillator, the controllable oscillator having a plurality of operational states, each of the plurality of operational states defining a distinct frequency for the output signal of the controllable oscillator, the computer readable medium comprising logic configured ~~to receive information associated with a predefined frequency,~~ to execute a binary search algorithm, to determine, based on execution of the binary search algorithm, the distinct frequency for the output signal of the controllable oscillator that best approximates ~~the~~ a predefined frequency, and to generate a control signal configured to change the controllable oscillator to the operational state corresponding to the distinct frequency that best approximates the predefined frequency.

26. (Previously presented) The computer readable medium of claim 25, wherein the logic is configured to enable switching between fine tune frequency control and coarse frequency control.

27. (Previously presented) The computer readable medium of claim 25, wherein the logic is further configured to change the controllable oscillator to the operational state corresponding to the distinct frequency that best approximates the predefined frequency.

28-31. (Canceled)